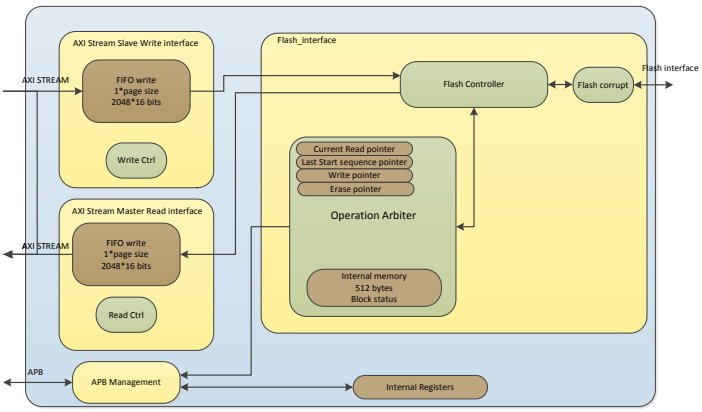
FEATURES

- Controller uses the NAND Flash memory as a non-volatile FIFO
- NAND Flash interface
- Write AXI-stream slave interface
- Read AXI-stream master interface
- 8-bit APB slave interface for dynamic configuration
- Special functionalities:
  - Erase of block managed by the controller, once data have been read with AXI-stream master interface
  - Read and Write pointer of the FIFO are kept in NAND Flash array during power off
  - Bad block management
  - NAND Flash bypass mode to connect Write AXI-stream interface to Read-AXI stream interface

- Specific operations (Self-Test, Format, Add a Bad Block and Fetch Failing block)
  - Up to 40 Mb/s write capability
  - Up to 350 Mb/s read capabililty



GENERAL DESCRIPTION

3DIPCC0736-1 is an IP memory controller intended to be used with the NAND Flash (1Gb x 8b) memory integrated into the 3D PLUS CMOS Space Camera modules: 3DCM739 (RGB sensor) and 3DCM734 (monochrome sensor).
This code brings the capability to store data provided by the sensor. It has been developed according to ECSS-Q-ST-60-02C ESA standard.

NAND FLASH INTERFACE PINOUT AND GENERICS

Name	Width	Direction	Functionality
SysClk	1	I	Main input clock used for all the RIMC except DFI interface
Rst_N	1	I	Input reset synchronous to SysClk, active LOW
APBI	1 record	I	APB slave input
APBO	1 record	O	APB slave output
AXI Stream interface			
AXIW_TVALID	1	I	Indicate a valid transfer from the master
AXIW_TREADY	1	O	Indicate that the slave accept the transfer
AXIW_TDATA	16	I	Payload data
AXIW_TLAST	1	I	Indicate a boundary
AXIW_TUSER	1	I	Define type of information in TDATA signal
AXIR_TVALID	1	O	Indicate a valid transfer from the master
AXIR_TREADY	1	I	Indicate that the slave accept the transfer
AXIR_TDATA	16	O	Payload data
AXIR_TLAST	1	O	Indicate a boundary
AXIR_TUSER	1	O	Define type of information in TDATA signal
Flash Nand interface			
R_B	1	I	Ready/busy
CE_N	1	O	Chip Enable
CLE	1	O	Command Latch Enable
ALE	1	O	Address Latch Enable
WE_N	1	O	Write Enable active low
RE_N	1	O	Read Enable active low
IO	8	I/O	8 bits of data from/to the Flash
WP_N	1	O	Write protect active low
Miscellaneous			
TEST_EN	1	I	This pin is used to activate or deactivate test functionalities

Table 1: NAND Flash memory controller interface pinout

Name	Functionality	Possible values
CLK_PERIOD	Type of memories	Between 13000ps and 62500ps
GSYNCRST	Type of internal reset	0: Asynchronous reset 1: Synchronous reset
VALIDATION	Enable generation of a block that can corrupt flash operation for validation purpose	0, 1
SIMU	Activated only for simulation. Used to accelerate simulation.	0, 1

Table 2: NAND Flash memory controller interface generics

RESOURCES

The 3DIPCC0736-1 IP core have been designed to maximize the operating frequency. Thus computational path are pipelined.

Table 3 provides FPGA ressources used by the 3DIPCC0736-1 IP core based on the following hypothesis :

- CLK_PERIOD = 13000
- GSYNCRST = 1
- VALIDATION = 0
- SIMU = 0

Core Cells	Block RAM
5102 (5%)	17 (15%)

Table 3: Occupancy rate of the FPGA

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