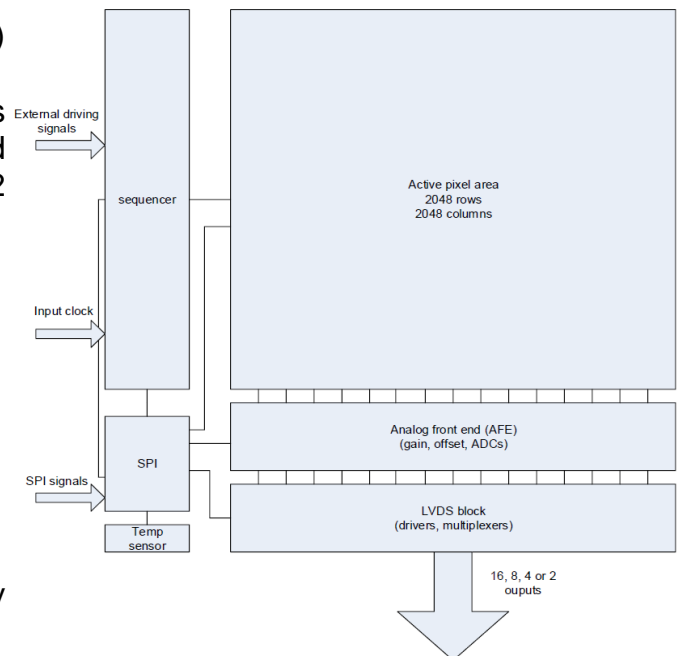


## FEATURES

- Generate frame requests and read-out the sensor
- Request and verify LVDS links calibration (synchronization of the receiving side with the LVDS outputs of the sensor)
- Frame rate:
  - 16 frames/s at full resolution (10-bit mode)
  - 7 frames/s at full resolution (12-bit mode)
- Low level image correction functionalities (defective pixels correction, background noise reduction) by implementing a 2x2 binning algorithm
- Ability to provide telemetry with:
  - The image itself
  - Integration time
  - Gain
  - Window position and size (X/Y offsets and width/height)
  - Test mode
  - Health status
  - Self-test
- Configuration of the following parameters by telecommand :
  - Integration time
  - Gain
  - Window position and size (X/Y offsets and width/height)
- Complete access to the SPI configuration registers of the sensor
- Ability to provide the sensor's temperature at a frequency of 1Hz by using the on-chip sensor



## GENERAL DESCRIPTION

3DIPCC0737-1 is an IP controller intended to be used with the CMOS sensor integrated into the 3D PLUS CMOS Space Camera modules: 3DCM739 (RGB sensor) and 3DCM734 (monochrome sensor). This code makes possible to get access to all the registers of the CMOS sensor. It has been developed according to ECSS-Q-ST-60-02C ESA standard.

## INTERFACE PINOUT

Name	Direction	Comments
SysClk	I	System clock
RST_N	I	Synchronous hardware reset, active low
ARst_N	I	Asynchronous hardware reset, synchronous to SysClk
FRAME_REQ	O	Frame request pin
SYS_RES_N	O	Sequencer reset of the sensor
T_DIG1_in	I	Test pin for digital signals (optional)
T_DIG2_in	I	Test pin for digital signals (optional)
T_DIG1_out	O	Test pin for digital signals (optional)
T_DIG2_out	O	Test pin for digital signals (optional)
T_EXP1_in	I	Program external exposure time (optional)
T_EXP2_in	I	Program external exposure time (optional)
T_EXP1_out	O	Program external exposure time (optional)
T_EXP2_out	O	Program external exposure time (optional)
OUT_CLK_P	I	LVDS positive clock channel
OUT_CLK_N	I	LVDS negative clock channel
OUTTX_P	I	LVDS positive data channel
OUTTX_N	I	LVDS negative data channel
OUTCTR_P	I	LVDS positive control channel
OUTCTR_N	I	LVDS negative control channel
CLK_OUT	O	Master clock for the sensor
LVDS_CLK_P	O	LVDS positive clock output
LVDS_CLK_N	O	LVDS negative clock output
TrDone	O	Training done. 1 clock cycle.
FrDone	O	Frame done. 1 clock cycle.

Axis_mi	I	AXI-Stream master input array
Axis_mo	O	AXI-Stream master output array
Ahbsi	I	AHB slave input array
Ahbso	O	AHB slave output array
Apbi	I	APB slave input
Apbo	O	APB slave output
SPI_CLK	O	SPI clock. This is the clock on which SPI runs
SPI_EN	O	SPI enable pin. When this pin is high the data should be written/read on the SPI
SPI_IN	O	Data output pin for the SPI interface the IP Core. The data to program the image sensor is sent over this pin
SPI_OUT	I	Data input pin. The data following a read action is sent to the sensor controller over this pin
OCD2V1	I	Over Current Detection on 2.1V
OCD3V3	I	Over Current Detection on 3.3V
PWR_SENS	O	Image sensor power

Table 1: Sensor interface pinout

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